IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A silicon wafer wherein stacking fault nuclei which are formed from agglomeration of interstitial silicon are distributed throughout [[the]] an entire in-plane direction of said silicon wafer, and a density of said stacking fault nuclei is set to a range of between $0.5\times10^{8}cm^{-3}$ and $1\times10^{11}cm^{-3}$.

2. (Previously presented) A silicon wafer according to claim 1, which is cut from an ingot formed from a perfect region wherein interstitial silicon-type point defect agglomerates and vacancy-type point defect agglomerates are substantially non-existent.

3. (Original) A silicon wafer according to claim 1, which is cut from an ingot formed from a region wherein vacancy-type point defects are dominant.

4.-5. (Canceled)

6. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer which manufactures [[the]] said silicon wafer according to claim 1, comprising:

vacancy heat treating for forming new vacancies in [[the]] an interior of said silicon wafer by means of a heat treatment of said silicon wafer in an atmosphere of gas containing nitrogen; and

SF nuclei heat treating [[which]] for agglomerates interstitial silicon released during precipitation of oxygen from vacancies injected by said vacancy ~~heat treatment step~~ treating, to form stacking fault nuclei,

~~and a temperature~~ wherein [[in]] said SF nuclei heat treating ~~is above 1100°C, and is increased at a rate of not more than~~ , a rate of temperature increase is set to 10°C/minute or less, a heat treatment temperature is set to 1100°C or higher, and said heat treatment temperature is maintained for one hour or more.

7. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer according to claim 6, wherein an oxide film on [[the]] a surface of said silicon wafer is removed prior to said vacancy heat treating.

8. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer according to claim 6, wherein during said vacancy heat treating, purging is conducted to remove oxygen from [[the]] said atmosphere of gas surrounding said silicon wafer, and said silicon wafer is quenched after said vacancy heat treating.

9. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[to the]] said silicon wafer according to claim 1, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

10. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 9.

11. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer according to claim 2, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

12. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 11.

13. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer according to claim 3, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

14. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 13.

15. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer manufactured by the method of claim 4, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

16. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 15.

17. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer manufactured by the method of claim 5, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

18. (Currently amended) A silicon wafer manufactured by [[the]] a method of claim 17.

19. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer manufactured by the method of claim 6, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

20. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 19.

21. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer manufactured by the method of claim 7, to form at least a defect-free layer on [[the]] said surface of said silicon wafer.

22. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 21.

23. (Currently amended) A ~~manufacturing~~ method [[of]] for manufacturing a silicon wafer comprising heat treating [[the]] said silicon wafer manufactured by the method of claim 8, to form at least a defect-free layer on [[the]] a surface of said silicon wafer.

24. (Currently amended) A silicon wafer manufactured by [[the]] said method of claim 23.

25. (New) A method for manufacturing a silicon wafer according to claim 6, wherein the method further comprises pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing said ingot to manufacture said silicon wafer,

wherein said ingot is pulled such that a ratio V/G of, a rate V at which said ingot is pulled, and a temperature gradient G of said ingot in a vertical direction in a vicinity of an interface between said silicon melt in said crucible and said ingot, is between $0.20mm^2/°C \cdot minute$ and $0.25mm^2/°C \cdot minute$.

26. (New) A method for manufacturing a silicon wafer according to claim 6, wherein the method further comprises pulling an ingot from a silicon melt in a crucible in accordance with the Czochralski method, and slicing said ingot to manufacture a silicon wafer,

wherein nitrogen is added while pulling said ingot, to set an internal nitrogen concentration within a range of between $5x10^{14}cm^{-3}$ and $5x10^{15}cm^{-3}$.

27. (New) A method for manufacturing a silicon wafer according to claim 6, wherein in said SF nuclei heat treating, while interstitial silicon is injected in a surface of said silicon wafer, said stacking fault nuclei are formed.

28. (New) A method for manufacturing a silicon wafer according to claim 6, wherein in said SF nuclei heat treating, said stacking fault nuclei are formed from only said interstitial silicon released during precipitation of oxygen.